REMARKS

By this response a new drawing sheet 22/24 comprising FIG. 22 has been submitted. Claims 1-12 and 20-28 remain pending, and no claim is presently amended or canceled. Reconsideration of the application is respectfully requested.

Submission of FIG. 22

Drawing sheet 22/24 comprising FIG. 22 as filed failed to specifically identify FIG. 22. This deficiency is overcome by the replacement sheet submitted herewith, and the Examiner's approval of the new drawing sheet is respectfully requested.

Rejections under 35 USC §102(e)

Claims 1-12 and 20-28 have been rejected under 35 USC §102(e) over Zheng, et al. (US Pub. 2003/166,318). Zheng recites the formation of a semiconductor device comprising forming an opening 18 in a base dielectric layer 16 and forming a lower electrode layer 20 (line 9, ¶[0012]) which typically covers the entire inner surface of container 18 (lines 1 and 2, ¶[0013]). A dielectric 22 is formed on the lower electrode 20, then a reoxidized layer 24 is formed over the dielectric layer 22 by subjecting the dielectric layer 22 to a reoxidation process (lines 14, 15 of ¶[0012]). Finally, an upper electrode layer 26, typically polysilicon, is formed over the reoxidized layer 24. FIG. 3 depicts an additional oxide layer (unnumbered) formed over the top electrode 26 and within opening 18.

Thus with regard to FIG. 2, Zheng recites the formation of two conductive layers (20, 26) and three dielectric layers (22, 24, unnumbered) in opening 18. Conductive layer 20 is a lower (bottom) electrode, and conductive layer 26 is an upper electrode. None of these layers forms a spacer. While Zheng does not detail the layout of the FIG. 3 cell (see ¶[0021], for example), with regard to FIG. 3 (reproduced and colored below), Zheng appears to recite the formation of only two sets of spacers: conventional dielectric spacers surrounding the transistor gates

(unnumbered, depicted in yellow and hatched from lower left to upper right, which are also depicted in FIGS. 1 and 2), and spacers (unnumbered, depicted in red and hatched from upper left to lower right) which add height to the plates. Zheng does not appear to specify whether the unnumbered spacers in red are dielectric or conductive. Assuming *arguendo* that the spacers depicted in red are conductive, they must form part of the capacitor bottom plate, at least because they physically contact layer 20 which Zheng calls the "lower electrode" (¶[0012], line 9).

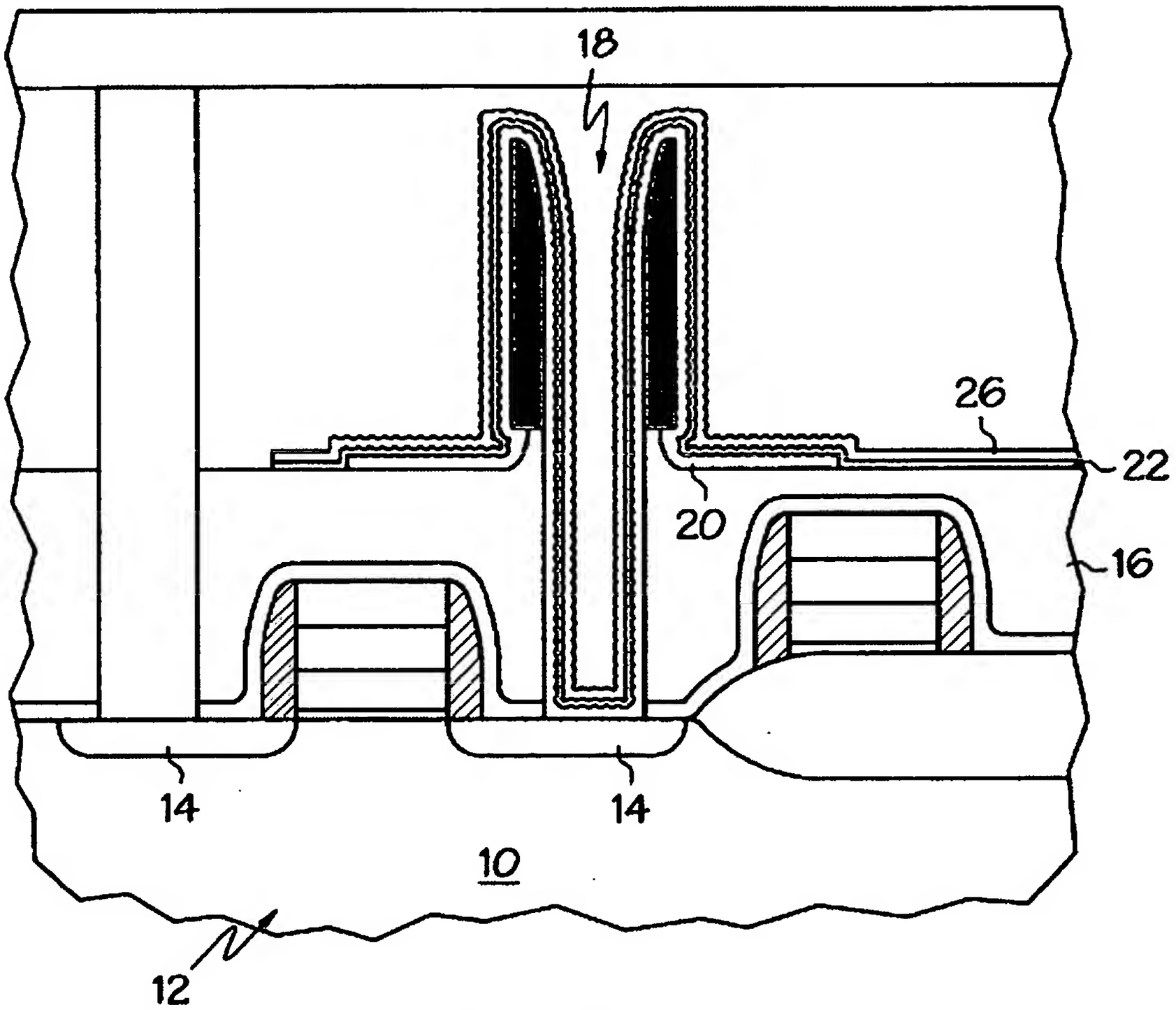

FIG. 3

The present invention as claimed recites novel and nonobvious differences over the invention of Zheng. Claim 1 recites "forming a first conductive cross-sectional spacer on said first dielectric sidewall wherein said first conductive spacer forms a portion of a capacitor top plate; forming a first capacitor cell dielectric layer

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on said first conductive spacer; forming a second conductive cross sectional spacer on said first capacitor cell dielectric layer; forming a first conductive layer on said second conductive spacer, wherein said second conductive spacer and said conductive layer each form a portion of a capacitor bottom plate; forming a second cell dielectric layer on said first conductive layer...and forming a conductive feature which electrically connects said first conductive spacer and said second conductive layer.

Zheng fails to teach or suggest "forming a first conductive cross sectional spacer wherein...wherein said first conductive spacer forms a portion of a capacitor top plate." Zheng either does not suggest a conductive spacer, or the conductive spacer is part of the bottom plate as discussed above. Zheng also does not teach or suggest forming a first capacitor cell dielectric layer on the first conductive spacer and "forming a second conductive cross sectional spacer on said first capacitor cell dielectric layer." Zheng forms no conductive spacer on any cell dielectric layer. Zheng forms the top plate to overlie the spacer in red, but the top plate is not formed as a spacer. As Zheng forms no second conductive spacer, it is not possible to form "a first conductive layer on said second conductive spacer."

Additionally, while the Examiner states that Zheng recites "a conductive feature (unlabeled) which electrically connects the first conductive spacer and the second conductive layer (FIG. 3)," the Examiner has not indicated what element of FIG. 3 is being used to teach this recitation. No element can be discerned in FIG. 3 of Zheng by the applicants' agent which fulfills the recitation of claim 1 of "forming a conductive feature which electrically connects said first conductive spacer and said second conductive layer." As it is not immediately obvious to which feature of Zheng the Examiner is referring, the applicants have not been given fair opportunity to reply.

The Examiner uses layer 20 of Zheng to teach the "top plate" of the present invention. However, layer 20 of Zheng is the lower (bottom) electrode (¶[0012], line 9). The Examiner uses some unspecified layer of Zheng as the bottom plate (page 3 lines 9-11), however the only capacitor cell layers in FIG. 2 which are conductive are layers 20 (the bottom electrode) and 26 (the top electrode). The Examiner uses both of layers 20 and 26 of FIG. 2 to teach the top electrode portions of the present invention, thus leaving the capacitor of FIG. 2 with no bottom plate. The Examiner further recites that FIG. 2 depicts "a first conductive cross sectional spacer on the first dielectric sidewall...[and] a second conductive cross-sectional spacer on the first capacitor cell dielectric layer." However, FIG. 2 depicts no conductive cross sectional spacers, and does not form a conductive spacer on the first capacitor cell dielectric layer 22. Clearly, the use of the features of Zheng as applied by the Examiner to teach the present invention as claimed is not reasonable and possible only in hindsight using the present claims as a blueprint, which is impermissible. The use of Zheng as applied by the Examiner is respectfully traversed, for example because it is not reasonable to use both the capacitor bottom and top plate of Zheng to teach the top plate of the present invention as claimed, and leave the storage capacitor of Zheng with no bottom plate.

Regarding claim 2, the Examiner states that Zheng discloses "prior to etching said base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer, and forming said first conductive cross sectional spacer to contact said third conductive layer." However, the Examiner has not indicated what is used in FIGS. 1 and 2 of Zheng to teach the third conductive layer formed over a planarized surface of the base dielectric layer prior to etching the base dielectric layer, and it does not appear that such a layer is taught, suggested, or depicted by Zheng at page 1 ¶[0012] and FIGS. 1-2 as stated by the Examiner.

Regarding claim 3, Zheng at best depicts two conductive cross-sectional spacers, specifically the red spacers at FIG. 3 as depicted above, which themselves may be dielectric spacers. Zheng does not discuss forming fourth and fifth conductive cross-sectional spacers at the location indicated by the Examiner, thus claim 3 is further allowable over the cited art as applied by the Examiner.

Regarding claim 4, Zheng does not appear to disclose forming a third conductive layer over a planarized surface of the base dielectric layer prior to etching the base dielectric layer as recited in claim 2 from which claim 4 depends, nor removing at least a portion of the third conductive layer using a planarizing process prior to forming the second cell dielectric layer.

The Examiner states that Zheng discloses various features of the present invention as claimed, but does not indicate what elements are being used to teach the recited features in such a way to make it possible to respond to the rejection in a meaningful way. For example, with regard to claim 5, the Examiner states that "Zheng discloses that the method of claim 4 further comprising removing a portion of each of said first conductive cross sectional spacer, said first capacitor cell dielectric layer, said second conductive cross-sectional spacer, and said first conductive layer during said planarizing process (page 1, paragraph [0012] and FIGS. 1-2)." However, at the specified location, Zheng does not discuss any planarizing process, specifically a planarizing process which removes "said first conductive cross sectional spacer, said first capacitor cell dielectric layer, said conductive cross-sectional spacer, and said first conductive layer." Further, layer 20 is not a conductive cross-sectional spacer," and it appears no conductive spacer exists in FIG. 1-2 of Zheng nor in paragraph [0012].

After a genuine attempt to respond to the rejections of the claims, it is submitted that a meaningful response to the assertions of the Examiner's office action is not possible as the office action fails to point out what is being used as a basis for rejection. As such, any response by the applicants' agent would be based merely on speculation, and would serve no useful purpose. It is further respectfully submitted that various other features of Zheng have been mischaracterized or misunderstood. For example, in ¶[0012] Zheng specifically states that layer 20 is the "lower electrode," while the Examiner states that layer 20 is "a portion of a capacitor top plate" (page 3 line 4). Further, it is apparent from FIG. 2 of Zheng and the text that layer 20 is not a spacer layer, but the Examiner uses layer 20 to teach a conductive spacer of the present invention as claimed.

A reading of the remaining independent claims with reference to Zheng shows at least the following differences between the present invention as claimed and the teachings of Zheng. The dependent claims are not discussed below, but may comprise differences which make them further allowable over the cited art which are not stated at this time. However, the dependent claims are allowable at least because they depend from allowable base claims.

It appears that Zheng fails to teach or suggest at least the following processing elements found in claim 9: providing a contact pad, forming an etch stop layer on the contact pad, forming a blanket planarized base dielectric layer on the etch stop layer; etching the conformal first conductive layer and the planarized base dielectric layer to form first and second cross sectional sidewalls in the base dielectric layer which define a recess in the base dielectric layer, wherein the etch exposes the etch stop layer; forming a second conductive layer which comprises a first conductive spacer on the first sidewall; forming a first cell dielectric layer on the etch stop layer; forming a third conductive layer on the first cell dielectric layer; spacer etching the third conductive layer and the first cell dielectric layer to form a second conductive spacer from the third conductive layer, to form a cell dielectric spacer from the first cell dielectric layer, and to expose the etch stop layer; subsequent spacer etching the third conductive layer and the first cell dielectric layer, etching the etch stop layer to expose the contact pad; forming a fourth conductive layer on the second conductive spacer and on the contact pad; forming a second cell dielectric layer on the fourth conductive layer; forming a fifth conductive layer on the second cell dielectric layer; and electrically connecting the first conductive spacer and the fifth conductive layer, wherein the second and fifth conductive layers form a first capacitor plate and the third and fourth conductive layers form a second capacitor plate interposed between the first conductive spacer and the fifth conductive layer.

It appears that Zheng fails to teach or suggest at least the following processing elements found in claim 20: within a recess in a base supporting layer, forming first and second conductive spacers having a first cell dielectric layer interposed therebetween which electrically isolates the first and second conductive spacers from each other; forming a first conductive layer electrically connected to the second conductive spacer within the recess; forming a first conductive layer electrically connected to the second conductive spacer within the recess; and electrically connecting the first conductive spacer and the blanket second conductive layer to form a storage capacitor, where the first conductive spacer and blanket second conductive layer form a portion of a capacitor top plate and the second conductive spacer and first conductive layer form a portion of a capacitor bottom plate.

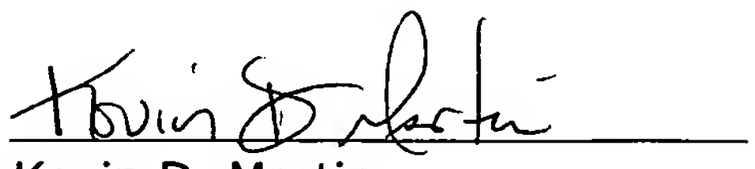
With regard to claim 25, it appears that Zheng fails to teach or suggest at least the following processing elements: forming a first cell dielectric layer to contact the first portion of the capacitor top plate; forming a first portion of a capacitor bottom plate comprising a vertically-oriented conductive spacer to contact the first cell dielectric layer; forming a second portion of the capacitor bottom plate comprising a vertically oriented layer to contact the first portion of the capacitor bottom plate; forming a second cell dielectric layer to contact the second portion of the capacitor bottom plate; forming a second portion of the capacitor top plate to contact the second cell dielectric layer and which comprises a portion which overlies the first portion of the capacitor top plate, the first and second cell dielectric layers, and the first and second portions of the capacitor bottom plate; and forming a conductive structure which electrically connects the first and second capacitor top plate portions.

It is therefore submitted that the office action is not sufficient to allow the applicants a fair reply, but that the above-stated differences demonstrate that the present claims are novel and nonobvious over Zheng, et al.

Conclusion

If there are any matters which may be resolved or clarified through a telephone call, the Examiner is cordially invited to contact the undersigned. This is believed to be a complete response to the Examiner's restriction requirement.

Respectfully submitted,



Kevin D. Martin
Agent for Applicant
Registration No. 37,882
Micron Technology, Inc.
PO Box 6
Boise, ID 83707-0006
Ph: (208) 368-4516
FAX: (208) 368-5606
e-mail: kmartin@micron.com

In the Drawings

A replacement sheet for FIG. 22, sheet 22/24, is being submitted herewith for the reasons discussed below in the "REMARKS."